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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/590,462	06/09/2000	Marco Racanelli	02SPE133P	1783

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EXAMINER	
DIAZ, JOSE R	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/590,462	RACANELLI ET AL.	
	Examiner	Art Unit	
	José R. Díaz	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,17-22,26-29 and 31-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,17-22,26-29 and 31-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 August 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3. Claims 1-2, 6, 9, 17-18, 20-21, 26-28, 29, 33 and 35-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US Pat. No. 5,880,516).

Regarding claims 1, 9, 26 and 35, Yamazaki teaches a method of forming a varactor device on a semiconductor substrate, comprising the steps of:

providing an epitaxial layer (3) situated in said semiconductor substrate (1), said semiconductor substrate having a first conductivity type (P) and said epitaxial layer having a second conductivity type (N) (see fig. 3);

providing an isolation structure (4) on said semiconductor substrate, said isolation structure defining an implant region (portions of the substrate not covered by isolation 4), said implant region being situated over said epitaxial layer (3) (see fig. 5A);

selecting a first peak dopant concentration and a first implant energy such that at least one of capacitance, leakage current, and tuning range of the varactor device is optimized (consider region 102 in figure 4A, and col. 2, lines 41-46);

forming a first implant (102) in said epitaxial layer using said first implant energy (see fig. 3), said first implant having said first peak dopant concentration (see fig. 4A) and said second conductivity type (N), wherein said first implant extends into said epitaxial layer a first distance (i.e. about 0.25 μm) (see col. 6, lines 14-15);

forming a second implant (103) in said epitaxial layer using a second implant energy (see fig. 3), said second implant having a second peak dopant concentration (see fig. 4A) and said second conductivity type (N), wherein said second implant extends into said epitaxial layer a second distance (i.e. about 0.5 μm) (see col. 6, lines 3-4),

wherein said second distance (i.e. about 0.5 μm) is greater than said first distance (i.e. 0.25 μm), and

wherein said second implant has a depth (i.e. about 0.5 μm) that is more than twice a depth of said first implant (i.e. about 0.25 μm) (see fig. 4A and col. 6, lines 3-4 and 14-15).

However, Yamazaki is silent with respect to performing the step of forming the second implant after the step of forming the first implant. It would have been obvious to

one of ordinary skill in the art to change the order of the method steps since it has been held that selection of any order of performing process steps is *prima facie* obvious in the absence of new or unexpected results. *In re Burhans*, 154 F.2d 690, 69 USPQ 330 (CCPA 1946).

Regarding claims 2 and 29, Yamazaki teaches annealing the device following the steps of forming said first implant and said second implant (col. 6, lines 20-23).

Regarding claims 6 and 33, Yamazaki further teaches selecting said second peak dopant concentration and said second implant energy such that the base resistance of the varactor device is minimized (col. 2, lines 41-46).

Regarding claims 17, 20, 27 and 36, Yamazaki further teaches the step of forming a contact layer of said first conductivity type (11) overlying said first implant (see fig. 3).

Regarding claims 18, 21, 28 and 37, Yamazaki further teaches that said first conductivity type and said second conductivity type are the same (consider the N-type buried layer (2) as the new substrate. See fig. 3).

4. Claims 4-5, 7-8, 31-32 and 34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US Pat. No. 5,880,516) in view of IBM Corporation (NN79013241), "Determination of Doping Profiles by Means of SIMS", IBM Technical Disclosure Bulleting, 1979, Vol. 21, Issue Number 8, p. 3241-3242.

Regarding claims 4-5, 7-8, 31-32 and 34, Yamazaki is silent with respect to using a secondary ion mass spectroscopy (SIMS) to determine the dopant concentration

profile. However, IBM Corporation (NN79013241) teaches that SIMS is a well-known technique use for determining doping concentrations and their respective depth (see last sentence of the "DISCLOSURE TEXT").

Yamazaki and IBM Corporation (NN79013241) are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to determine the dopant concentration profile of the first and second implants by using secondary ion mass spectroscopy (SIMS). The motivation for doing so, as is taught by IBM Corporation (NN79013241), is determining the doping profile of the wafer (see lines 1-3 of the "DISCLOSURE TEXT"). Therefore, it would have been obvious to combine IBM Corporation (NN79013241) with Yamazaki to obtain the invention of claims 4-5, 7-8, 31-32 and 34.

5. Claims 19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamazaki (US Pat. No. 5,880,516) in view of Wiedmann (US Pat. No. 3,770,519).

Regarding claims 19 and 22, Yamazaki (US Pat. No. 5,880,516) is silent with respect to providing a CMOS well as an isolation structure. Wiedmann teaches that is well known in the art to form CMOS well (4) as isolation structures.

Yamazaki and Wiedmann are analogous art because they are from the same field of endeavor as applicant's invention. At the time of the invention it would have been obvious to a person of ordinary skill in the art to provide an isolation structure comprising a CMOS well. The motivation for doing so, as is taught by Wiedmann, is

isolating diodes from each other without requiring the allocation of additional substrate space for isolation purposes (col. 2, lines 23-27). Therefore, it would have been obvious to further combine Wiedmann with Yamazaki to obtain the invention of claims 19 and 22.

Response to Arguments

6. Applicant's arguments with respect to claims 1-2,4-9,17-22,26-29 and 31-37 have been considered but are moot in view of the new grounds of rejection.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Gomi (US Pat. 5,010,026) teaches a bipolar transistor in figure 1; Hans et al. (US Pat. No. 3,581,164) teaches a varactor in figure 1; and Nagase (JP 04092477 A) teaches a varactor in figure 1H.

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

Any inquiry concerning this communication or earlier communications from the examiner should be directed to José R. Díaz whose telephone number is (571) 272-1727. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JRD
11/15/04

Tom Thomas